ES_LPC1768

Errata sheet LPC1768

Rev. 3 — 1 July 2010 **Errata sheet**

Document information

Info	Content
Keywords	LPC1768 errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table at the end of the document.

Revision history

Rev	Date	Description
3	20100701	• Added RTC.1.
2	20100316	• The format of this errata sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Added I2S.1 and Ethernet.1.
1	20091014	• Added MCPWM.1

Contact information

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1. Product identification

The LPC1768 devices typically have the following top-side marking:

LPC1768xxx

xxxxxxx

xxYYWWR[x]

The last/second to last letter in the third line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the LPC1768:

Table 1. Device revision table

Revision identifier (R)	Revision description
'-'	Initial device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

2. Errata overview

Table 2. Functional problems table

Functional problems	Short description	Revision identifier	Detailed description
RTC.1	The Real Time Clock (RTC) does not work reliably within the temperature specification.	'-'	Section 3.1
I2S.1	XY divider will not work for PCLK-I2S higher than 74 MHz	'-'	Section 3.2
Ethernet.1	Ethernet TxConsumeIndex register does not update correctly after the first frame is sent	'-'	Section 3.3
PLL0.1	PLL0 (Main PLL) remains enabled and connected in Deep Sleep and Power-down modes	'-'	Section 3.4
PCLKSELx.1	Peripheral Clock Selection Registers must be set before enabling and connecting PLL0	'-'	Section 3.5
MCPWM.1	Input pins (MCI0-2) on the Motor Control PWM peripheral are not functional	'-'	Section 3.6

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

3. Functional problems detail

3.1 RTC.1: The Real Time Clock (RTC) does not work reliably within the temperature specification

Introduction:

The RTC is a set of counters for measuring time when system power is on, and optionally when it is off. The RTC is clocked by a separate 32 kHz oscillator that produces a 1 Hz internal time reference. The RTC is powered by its own power supply pin, VBAT, which can be connected to a battery, externally tied to a 3 V supply, or left floating. The RTC can operate over temperature range from −40 °C to 85 °C.

Problem:

The RTC does not work reliably within the temperature specification.

Work-around:

None.

3.2 I2S.1: The XY divider (8-bit Fractional Rate Divider) will not work for PCLK_I2S (Peripheral clock for I2S) higher than 74 MHz

Introduction:

The transmitter/receiver MCLK (Master clock output) rate is generated using a fractional rate generator, dividing down the frequency of PCLK_I2S. Values of the numerator (X) and the denominator (Y) must be chosen to produce a frequency twice that desired for the receiver MCLK, which must be an integer multiple of the receiver bit clock rate.

Problem:

The XY divider (8-bit Fractional Rate Divider) will not work for PCLK_I2S (Peripheral clock for I2S) higher than 74 MHz.

Work-around:

Do not use PCLK_I2S signal higher than 74 MHz.

3.3 Ethernet.1: Ethernet TxConsumeIndex register does not update correctly after the first frame is sent

Introduction:

The transmit consume index register defines the descriptor that is going to be transmitted next by the hardware transmit process. After a frame has been transmitted hardware increments the index, wrapping the value to 0 once the value of TxDescriptorNumber has been reached. If the TxConsumeIndex equals TxProduceIndex the descriptor array is empty and the transmit channel will stop transmitting until software produces new descriptors.

Problem:

The TxConsumeIndex register is not updated correctly (from 0 to 1) after the first frame is sent. After the next frame sent, the TxConsumeIndex register is updated by two (from 0 to 2). This only happens the very first time, so subsequent updates are correct (even those from 0 to 1, after wrapping the value to 0 once the value of TxDescriptorNumber has been reached)

Work-around:

Software can correct this situation in many ways; for example, sending a dummy frame after initialization.

3.4 PLL0.1: PLL0 (Main PLL) remains enabled and connected in Deep Sleep and Power-down modes

Introduction:

If the main PLL (PLL0) is enabled and connected before entering Deep Sleep or Power-down modes, main PLL (PLL0) automatically turns off and disconnects after the chip enters Deep Sleep mode or Power-down mode leading to reduced power consumption.

Problem:

If the main PLL (PLL0) is enabled and connected before entering Deep Sleep or Power-down modes, it will remain enabled and connected after the chip enters Deep Sleep mode or Power-down mode causing the power consumption to be higher.

Work-around:

In the software, user must disable and disconnect the main PLL (PLL0) before entering Deep Sleep and Power-down modes to reduce the power consumption. This must be done only if the main PLL (PLL0) was enabled and connected before entering Deep Sleep mode or Power-down mode.

The code below demonstrates the steps to disable and disconnect the main PLL0:

```
PLL0CON &= ~(1<<1);                    /* Disconnect the main PLL (PLL0) */

PLL0FEED = 0xAA;                       /* Feed */

PLL0FEED = 0x55;                       /* Feed */

while ((PLL0STAT & (1<<25)) != 0x00); /* Wait for main PLL (PLL0) to disconnect */

PLL0CON &= ~(1<<0);                    /* Turn off the main PLL (PLL0) */

PLL0FEED = 0xAA;                       /* Feed */

PLL0FEED = 0x55;                       /* Feed */

while ((PLL0STAT & (1<<24)) != 0x00); /* Wait for main PLL (PLL0) to shut down */

/************** Then enter into Deep sleep mode or Power-down mode*****************/
```

3.5 PCLKSELx.1: Peripheral Clock Selection Registers must be set before enabling and connecting PLL0

Introduction:

A pair of bits in the Peripheral Clock Registers (PCLKSEL0 and PCLKSEL1) controls the rate of the clock signal that will be supplied to APB0 and APB1 peripherals.

Problem:

If the Peripheral Clock Registers (PCLKSEL0 and PCLKSEL1) are set or changed after PLL0 is enabled and connected, the value written into the Peripheral Clock Selection Registers may not take effect. It is not possible to change the Peripheral Clock Selection settings once PLL0 is enabled and connected.

Work-around:

Peripheral Clock Selection Registers must be set before enabling and connecting PLL0.

3.6 MCPWM.1: Input pins (MCI0-2) on the Motor Control PWM peripheral are not functional

Introduction:

On the LPC1768, the Motor Control PWM (MCPWM) peripheral is optimized for three-phase AC and DC motor control applications and can also be used in applications which require timing, counting, capture, and comparison. The MCPWM contains three input pins (MCI0-2) for PWM channels 0, 1, and 2. The inputs can be used as feedbacks for controlling brushless DC motors with Hall sensors, and also can be used to trigger a Timer/Counter's (TC) capture or increment a channel's TC when MCPWM is configured as a timer/counter.

Problem:

The input pins (MCI0-2) are not functional.

Work-around:

The GPIO interrupts on port 0 or port 2 can be used instead of the MCPWM MCI0-2 pins. The GPIO interrupts give the ability to trigger an interrupt on both the rising and falling edge; therefore, all six states of the connected hall sensor can be detected through an interrupt.

4. AC/DC deviations detail

4.1 n/a

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